REMARKS

This paper is responsive of an Office Action mailed on September 20, 2005. Prior to this response claims 1-13 and 27-28 were pending. Claims 1-13 and 27-28 remain pending.

Claims 1-13 and 27-28 have been rejected under 35 U.S.C. 102(e) as anticipated by Huotari (US Pub 2004/0106249). The Office Action states that Huotari describes all the limitations of claims 1, 27, and 28. This rejection is traversed as follows.

The priority date for the Huotari application is December 3, 2002, based upon Provisional Application 60/430,960. To "swear behind" Huotari's priority data, the Applicant has enclosed, as Attachment A, the declaration of Wei Goa, one of the co-inventors of the instant application. In his declaration, Mr Goa swears that the subject matter of the instant application claims were conceived of, and reduced to practice prior to the date of December 3, 2002.

Attachments B and C are enclosed to support Mr. Goa's assertions. Attachment B is a true copy of the patent disclosure that was submitted to the Sharp Laboratories of America (SLA) Patent Department. The instant application was authorized as a result of the patent disclosure. The patent disclosure includes a figure on page 4 of a gate electrode comprising a gate dielectric, a barrier metal overlying the dielectric, and a gate metal overlying the barrier metal. Some examples of barrier metals are mentioned in Section 10(2). Gate metals are discussed in Section 10(3). Section 10(4), under the figure, states that the thinness of the barrier metal precludes it from having an affect on the gate electrode work function.

Attachment C is a true copy of a monthly report submitted by Wei Goa to his supervisor (and co-inventor) Yoshi Ono. Table 2 (incorrectly

marked as "Table 1") and the accompanying description discuss the measured work function of various gate electrode stacks (gate metal/barrier layer). For example, shown in the Table are Pt/TaN and Nb/TaN stacks. Further, page 1 of the report discusses the work function of Pt/TiN and Ir/TiN stacks. The monthly report clearly shows that the claimed invention was reduced to practice. In his declaration, Mr. Goa swears that this reduction to practice occurred prior to December 3, 2002.

Since claims 1-13 and 27-28 were conceived of, and reduced to practice prior to the priority date of the prior art reference, the Application respectfully requests that the rejection be withdrawn.

It is believed that the application is in condition for allowance and reconsideration is earnestly solicited.

Respectfully submitted,

Date: 12/19/2005

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ATTACHMENT A

DECLARATION OF WEI GAO UNDER 37 CFR 1.131

I, Wei Gao, hereby declare as follows:

1. My residence address is 2402 SE 180th CT, Vancouver, WA 98683.

2. Since April 2001, I have been employed by Sharp Laboratories of America, Inc. (SLA), 5750 N.W. Pacific Rim Blvd., Camas, WA 98607.

3. I am a co-inventor of Patent Application Serial No. 10/784,662, and I invented the device recited in amended claims 1-13 and 27-28 prior to December 3, 2002.

4. Attachment B is a true copy of the SLA patent disclosure document filed with the SLA Patent Department. I affirm that the patent disclosure document was written, signed, and witnessed before December 3, 2002. The disclosure shows the concept of a gate electrode having a first metal barrier layer, with an overlying second metal, where the first metal layer is thin enough so as to not effect the overall work function of the gate electrode.

5. Attachment C is a true copy of weekly report describing the results of experiments conducted in the laboratory. The report shows a first metal buffer layer of TiN, TaN, or Ti, having a thickness in the range of 1 to 200 nanometers (nm). The overlying second metal layer is Al, Nb, or Pt. The lab results and write clearly show a reduction to practice of the claimed invention.

6. I hereby declare that all statements made herein of my

own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United State Code and that such willful, false statements may jeopardize the validity of the application or patent issuing thereon.

12/5/2005 _____

Date Wei Gao

ATTACHMENT B

SHARP Laboratories of America, Inc.
5750 NW Pacific Rim Boulevard
Camas, Washington 98607

SLA Confidential

SLA Docket No. 674

1. **Descriptive Title of Invention:** Method for using reactive materials as gate electrodes

2. **Inventor(s):**

Full Name:	John	F.	Conley, Jr.			
	First	Middle	Last			
Address:	701 NE 124th Ave.	Vancouver	WA	98684	Clark	
	Street	City	State	Zip	County	
Citizenship:	USA					
Telephone:	360/907-0570 Home	360/834-8668 Company				

Inventor(s): Full Name:	Yoshi		Ono			
	First	Middle	Last			
Address:	2526 NW 24th Circle	Camas	WA	98607	Clark	
	Street	City	State	Zip	County	
Citizenship:	USA					
Telephone:	360/834-7060 Home	360/834-8582 Company				

Inventor(s): Full Name:	Wei		Gao			
	First	Middle	Last			
Address:	2402 SE 180th Ct.	Vancouver	WA	98683	Clark	
	Street	City	State	Zip	County	
Citizenship:	P.R. China					
Telephone:	360/882-1086 Home	360/834-8781 Company				

Supervisor's Acknowledgment: "I believe this disclosure is novel and complete and should be submitted to the Patent Review Committee."

Supervisor's Signature: [redacted]

Date: [redacted]

Supporting Group ☐ CRDG ☐ AVSG ☐ CSG ☐ ISG ☐ DSG

☒ ICG ☐ LCDG ☐ Other:

3. **Project & Supervisor:**

Inventor Signature [redacted] Date

Inventor Signature [redacted] Date Witnessed & Understood By [redacted] Date

Inventor Signature [redacted] Date Witnessed & Understood By [redacted] Date

SHARP Laboratories of America, Inc.
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Camas, Washington 98607

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SLA Docket No. 674

Supervisor's Name: Sheng Teng Victor Hsu

Supervisor's Title: Director, IC Process Technology

Project Number/Name:

4. Conception of the Invention:

Date Conceived: [redacted]

Date of first Written Description: [redacted]

Notebook & Page No. or File Archive: Notes for Quarterly Review Meeting

Date first explained to others (whom?): [redacted]

Planned Application for the Invention:

5. Construction & Test of First Prototype Embodying the Invention:

Date First Prototype Completed:

Part Number/Product Description:

Date of First Successful Test:

Successful Operation Witnessed By:

6. Public Disclosure of Invention (Presentation at public meeting or publication) (NOTE: Patent Application MUST be filed prior to any public disclosure.):

Date of First Public Disclosure:

Setting (Conference/Journal Name):

Title of Paper or Presentation:

Type of Disclosure (Written/Verbal):

Does Data Sheet or Application Note Disclose the Invention (when)?

7. What is the field of the invention (invention relates to...):

This invention relates to integrated circuit fabrication and control of MOSFET device characteristics.

8. What is the problem solved by your invention? How is it solved in the prior art (do not put search pages here)?

Doped polysilicon has been the gate material of choice for the last several generations of microelectronics technology. To achieve low Vth devices (required for high performance), p+ poly is used for PMOS and n+ poly is used for NMOS. As devices are scaled, the thickness of the poly-Si gate is decreased. In order to maintain low sheet resistance and a large effective oxide capacitance (i.e. minimize poly depletion effects) it

Inventor Signature [redacted] Date [redacted]

Inventor Signature [redacted] Date [redacted] Witnessed & Understood By [redacted] Date [redacted]

Inventor Signature [redacted] Date [redacted] Witnessed & Understood By [redacted] Date [redacted]

has been necessary to increase poly doping density with each successive generation. This has led to the problem of channel autodoping in which B from the gate poly diffuses across the thin gate dielectric and into the channel, causing Vth variations which degrade device performance.

In order to solve the problems of gate resistance, poly-depletion, and B-diffusion, the industry soon will be forced to switch to metal gate electrodes. To achieve acceptable Vth, metal gate materials with the correct work function will be necessary. This implies one metal for NMOS and a different metal for PMOS. Thus, dual metal (with work functions corresponding to p+ and n+ poly Si) will be required for CMOS circuits.

It has been shown that many of the desirable metal materials have adhesion and/or stability problems when placed in direct contact with the SiO_2 or high k gate dielectrics (HfO_2, ZrO_2, etc.). For example, it is known that Pt does not adhere well to SiO_2 and metals such as Ti, Hf, Zr, etc. scavenge O, reducing the underlying dielectric film, causing degradation and increased leakage.

This method will enable the use of certain metal and dielectric combinations for the manufacture of integrated circuits.

9. **How is your solution different from the prior art (one paragraph or list)?**

Metal gates will be needed in future MOS devices. In previous work, metals have been placed in direct contact with the gate dielectric (SiO2 or high-k) and revealed adhesion and stability issues (reactivity of metal with dielectric leading to oxygen scavenging)

We disclose the use of a thin interfacial layer / barrier to 1) improve adhesion between metal gate and dielectric and / or 2) serve as a barrier metal to reduce reactivity. A key element is that, based on an earlier SLA disclosure (W. Gao and Y. Ono), as long as the thickness of this interfacial metal is < ~50A, it will not impact Vth of the transistor. Because the barrier / layer is a metal, gate resistivity will not be adversely impacted.

Inventor Signature [redacted] Date [redacted]

Inventor Signature [redacted] Date [redacted] Witnessed & Understood By [redacted] Date [redacted]

Inventor Signature [redacted] Date [redacted] Witnessed & Understood By [redacted] Date [redacted]

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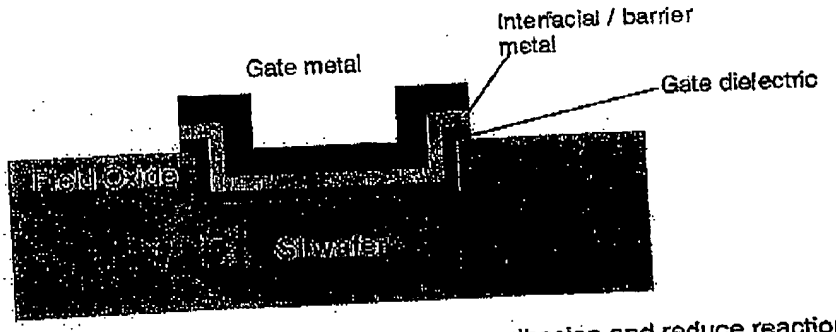
10. Please give a detailed description of your invention, include any graphics, notebook pages or other material necessary to understand your invention.

(1) The structure prior to depositing the barrier layer is formed by any state of the art method. The example shown in the figure is for the gate replacement process. A gate dielectric of any kind has been deposited / grown and is ready for the metal gate.

(2) A thin barrier / interfacial layer of metal of desired thickness (< 50A) is deposited by any state of the art method. Depending on the structure, this metal material can be TiN, TaN or WN.

(3) A metal gate with the desired workfunction / properties is then deposited to desired thickness by any state of the art method. Depending of the design of the structure, this film can be Pt, Ti, Hf, Zr, or any other potential metal or metal compound.

(4) The metal stack is then etched or CMP'd to form the device structure desired. The structure can then be treated thermally, electrically, or mechanically, as required.



The barrier / interfacial metal should improve adhesion and reduce reaction between the overlying gate and the underlying dielectric. Because the interfacial layer is <~50A, the workfunction of the resulting device should be determined solely by the top gate metal.

11. What other embodiments or examples are there of your invention?

We envision that potentially, a gate stack consisting of any gate metal and any dielectric could be made compatible, providing a suitable barrier metal can be found.

In another embodiment, should the workfunction of the metal gate not be an optimum value, the proper thickness of the intermediate layer, typically greater than 90Å can be used to shift the threshold voltage to the desired value. This is in accordance to the previously disclosed invention (2).

Inventor Signature [redacted] Date [redacted] Witnessed & Understood By [redacted] Date [redacted]

Inventor Signature [redacted] Date [redacted] Witnessed & Understood By [redacted] Date [redacted]

Inventor Signature [redacted] Date [redacted]

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Camas, Washington 98607

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SLA Docket No. 674

12. List related publications, patents, articles, or other references and give a brief summary (Indicate the extent of your search, attach search pages, if any):

1. V. Misra, G.P. Heuss, H. Zhong, "*Use of metal-oxide-semiconductor capacitors to detect Interactions of Hf and Zr gate electrodes with SiO_2 and ZrO_2*," Appl. Phys. Lett. **78**, 4166 (2001).

2. W. Gao and Y. Ono, "MOSFET threshold voltage tuning with metal gate stack control," SLA Patent Disclosure, [redacted]

3. V. Misra, M. Kulkarni, G. Heuss, H. Zhong, and H. Lazar, "*Electrical and Material Properties of Metal Silicate Dielectrics and Metal Gate Electrodes for Advanced CMOS Devices*," in Electrochemical Society Proceedings Vol. 2000-9, p. 291-98 (2000).

Inventor Signature [redacted] Date [redacted] Witnessed & Understood By [redacted] Date [redacted]

Inventor Signature [redacted] Date [redacted] Witnessed & Understood By [redacted] Date [redacted]

Inventor Signature

ATTACHMENT C

Sharp Labs of America

To: Yoshi Ono
From: Wei Gao
cc: Group Files
Date: [redacted]
Subject: [redacted]

Single metal gate lot 3

Single metal gate lot 3 has gone through radical gate oxidation and RTA. The detailed information is listed in table 1 and the lot is at contact etch and is going to be ready for measurement soon.

Table 1. Radical oxidation parameter and RTA anneal

	Wafer temperature	Time(min)	Measured oxide thickness
Radical oxidation	200°C	8	29Å
RTA(MPT)	750°C	1	27Å

Dual metal gate project

PVD TaN using 50%N_2/Ar produced in our lab has show its stability with SiO_2 up to high temperature. However, the workfunction of this material is not stable even after 450°C anneal. From workfunction tuning point of view, Pt/TiN or Ir/TiN should provide big enough V_{fb} shift although the work function does not lineup with Si bandgap very well. However, our TiN is known to be oxidized at elevated temperature, and we don't have good enough furnace to anneal the device without oxidizing them. In order to try our TiN stack with Pt, we put 2000Å Al on top of Pt(1200Å)/TiN to see the effect of workfunction tuning before/after anneal, the result is showing in Figure 1.

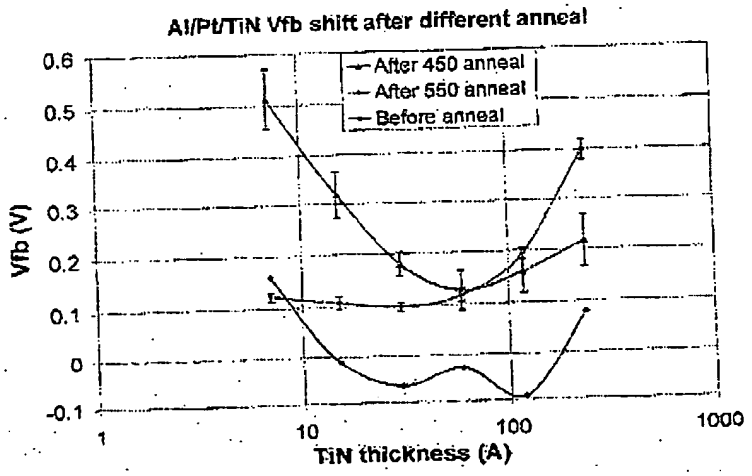

Figure 1 shows that before anneal, Al/Pt/TiN stack shows a scattered result. Not only the curve goes up and down, the error bar is also too big to put on the graph. After 450°C anneal, V_{fb} shows an smooth change up to 60Å and goes the other way after that. The V_{fb} change is around 0.4V. After 550°C anneal, the curve further changed which could be attributed to the involvement of Al since Al could diffuse through Pt. On the left, (7Å point), work function of Pt seems greatly dropped (because of the Al) and on the other side, the work function of 236Å TiN increased for some other unknown reason. Besides all this dramatic changes, the C_{acc} is observed to have certain change but the capacitor doesn't fail and the change is limited.

So far we have tested several workfunction tuning material combinations based on our dual metal gate configuration. Table 2 summarize the result we got so far.

Table 1. Summary of workfunction tuning experiments

stack	Transition region	V_{fb} shift (V) as deposited	After 450°C anneal (v)	C_{acc}	Possible reason
Al/TiN	100 Å	0.6	0.5	Not stable	Al/SiO_2
Pt/Ti	40 Å	0.9	0.9	Not stable	Ti/SiO_2
Pt/TaN*	100 Å	N/A	0.25	Not stable	Ta/SiO_2
Al/TaN*	100 Å	N/A	0.3	Not stable	Ta/SiO_2 and Al
Al/TaN**	50 Å	0.75	N/A	Stable	TaN/SiO_2 is stable
Nb/TaN**	100 Å	0.8	0.3	Stable	workfunction of TaN
Al/Nb/TaN**	100 Å	0.8	0.2	Stable	is not stable
Al/Pt/TiN	60 Å	N/A	0.4	Stable	Al involvement

* Ta rich PVD TaN using 15%N_2/Ar
** N rich PVD TaN using 50%N_2/Ar

From this table we can see the first 4 experiment proves that the dual metal gate stack require both metal to be stable when contact with SiO_2. and the next 4 experiment shows that the stack is stable with SiO_2, however, the workfunction properties of the stack is not stable during anneal. As good barrier layer or adhesion enhancer, TaN and TiN all have multiple valence states which allows them to form many nitrides with different stoichiometries, PVD, on the other hand, generates meta-stable film structure which allows flexibility to change easily during anneal.

Besides the stability issue, the sputtering process always causes gate dielectric thinning as well as introducing charges, the loss becomes bigger when the gate dielectric is getting very thin and the extra charge introduced may require unnecessary treatment than there is not. Generally speaking, CVD or ALD is more preferred process when work with gate dielectric.

We have decided to try CVD TaN on our CVC system and literature search was carried out. Since there are only a few published research on CVD or ALD TaN, I listed the major feature of different approaches into the following table.

From the details listed in the table, the following conclusion could be drawn:

1. From barrier properties point of view, CVD or ALD TaN is preferable. However, the film densities are normally lower (<10) which require post deposition anneal for densification and stabilization. PVD TaN has higher density (>10) but still lower than 16.6, the theoretical value.
2. As a workfunction tuning material, it has to be stable and high density, as deposition method, the substrate temperature has to be lower than 430°C (to fit in CVC system and not to interfere with our existing process). Judged by this two categories, TBTDET ALD is no good because the deposition temperature has to be <260°C and the film has low density. PEALD TBTDET can produce higher density film under 260°C, however, it

requires modification of our CVC tool (add plasma system). Y. H. Kim et al used CVD TBTDET to produce TaN that is stable up to 1000°C, however, the deposition temperature is 600°C followed by 700°C anneal in NH_3.

3. Tantalum halide (Cl and Br) were studied to deposit TaN as the candidate of Cu barrier layer three years ago, due to the bonding strength difference, $TaCl_5$ require >600°C deposition temperature in order to get low resistivity, while $TaBr_5$ require only 350-425°C. The film deposited from CVD $TaBr_5$ contains <2% O and <0.5%Br, the film is amorphous $TaN_{1.83}$ and its resistivity is normally higher.
4. Because of the constrain on deposition temperature, CVD $TaBr_5$ becomes the only approach that could fit in to our current CVC system.
5. It seem CVD $TaBr_5$ could produce so far the purest TaN at low temperature compare with other ALD or CVD methods. As a Cu barrier material it fails at above 550°C due to the fast boundary diffusion when the film turns from amorphous to microcrystalline. For our dual metal gate project, this may not be a problem. The major questions for $TaBr_5$ produced TaN are its resistivity, its workfunction, and workfunction thermal stability.

Table 2. Comparison of different deposition approaches for TaN film

	CVD $TaBr_5$	CVD $TaCl_5$	PEALD TBTDET	CVD TBTDET	ALD TBTDET	PVD sputtering
Deposition temperature	350-425°C	>600° C.	260°C	600°C d. 700°C a.	<260°C[1]	300°C
ΔH (kcal/mol)	-143	-205				
Reducing agent	$H_2 + NH_3$		H_2		NH_3	
Crystal phase	$TaN_{1.83}$ [2] amorphous		Poly	TaN [3]	amorphous	$TaN_{1.71}$[2] poly
Density	9.7[2]		7.9[1]		3.6[1]	~13[0], 10.17[2]
Contamination	<2%O		15-35%C and O	1.5%C, <1%O[3]	Significant amount	
ρ(μΩcm)	2500		400			~400
Thermal stability	< 550°C			1000°C		<650°C[2]
Step coverage	90% at 8:1 0.13μm		100% at 10:1 0.3μm			Poor
Major drawbacks		High temp.	Slow proc cmplx sys.	High temp.	Low den. aging eff.	Step coverage

[0] Our PVD data.
[1] J-S Park, H-S Park and S-W Kang, ***J Elec.Chem.Soc.*** 149(2002)C28
[2] A. E. Kaloyeros et al. ***J Elec.Chem.Soc.*** 146(1999)170
[3] Y. H. Kim, et al., ***IEDM*** 2001

ATTACHMENT D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		Attorney Docket: SLA0674
Inventor:	John F. Conley, Jr., et al.	Confirmation No. 2287
Serial No.:	10/784,662	Group #: 2815
Filed:	February 23, 2004	Examiner: Edward J. Wojciechowicz
Title:	REACTIVE GATE ELECTRODE CONDUCTIVE BARRIER	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

ASSOCIATE POWER OF ATTORNEY

CHANGE OF CORRESPONDENCE ADDRESS

I hereby appoint Gerald Maliszewski, P. O. Box 270829 San Diego, CA 92198-29, U. S. Patent and Trademark Office Registration Number 38,054, as an associate attorney for the above-captioned matter, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Please change the Correspondence address to that associated with Customer Number 55,286.

Respectfully submitted,

Date: 12/19/05

David C. Ripma, Registration # 27,672

David C. Ripma Patent Counsel
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5750 N.W. Pacific Rim Highway
Camas, WA 98607
Phone: (360) 834-8754
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